AMENDMENTS TO THE CLAIMS:

If entered, this listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1-28 (Canceled)

29. (Currently Amended) A stacked gate memory cell pair having a graded doubly diffused drain (DDD) profile exhibiting minimum disturb voltage difference comprising:

a semiconductor substrate of a first conductivity type having active and passive regions defined and having a top surface;

a pair of stacked gates overlying the substrate surface, each said stacked gate having a gate oxide layer overlying the substrate, a floating gate layer overlying the gate oxide layer, an inter-gate oxide layer overlying the floating gate, a control gate overlying the inter-gate layer, sidewall spacers conforming to said stacked gates;

source regions of a second conductivity type formed within said substrate and adjacent to each of said stacked gates;

a common drain region of a second conductivity type formed within said substrate and defined between each pair of said stacked gates;

channel regions within said substrate lying beneath said stacked gates and defined between said source regions and said common drain region;

a heavily doped implanted region within said common drain region;

a lightly doped implanted region beneath and surrounding said heavily doped implanted region wherein said lightly doped and said heavily doped implanted regions are smoothly graded doping profiles that extend from said common drain region toward the center of said channel region, wherein said smoothly graded doping profiles are defined by tilt angle impurity implantation and minimal thermal diffusion, wherein said source regions are formed prior to said tilt

angle impurity implantation and said source regions are masked from said tilt angle impurity implantation, and wherein said smoothly graded doping profiles provide minimal inter-memory cell disturb voltage difference.

30. (Previously Presented) A stacked gate memory cell pair of Claim 29, wherein said lightly doped implanted region comprises phosphorous ions at a dosage level between about $1x10^{13}$ to $5x10^{13}$ atoms/cm^3.

31. (Previously Presented) A stacked gate memory cell pair of Claim 29, wherein said heavily doped implanted region comprises arsenic ions at a dosage level between about $1x10^{15}$ to $5x10^{15}$ atoms/cm^3.

32. (Previously Presented) A stacked gate memory cell pair of Claim 29, wherein said minimal inter-memory cell disturb voltage difference is about |0.18V|.

33. (Previously Presented) A stacked gate memory cell pair of Claim 29, wherein said gate oxide layer has a thickness of between about 80 to 95 Å.

34. (Previously Presented) A stacked gate memory cell pair of Claim 29, wherein said floating gate has a thickness of between about 1000 to 2000 Å.

35. (Previously Presented) A stacked gate memory cell pair of Claim 29, wherein said inter-gate oxide layer has a thickness of between about 120 to 160 Å.

36. (Previously Presented) A stacked gate memory cell pair of Claim 29, wherein said control gate has a thickness of between about 1500 to 2000 Å.

37. (Previously Presented) A stacked gate memory cell pair of Claim 29, wherein said sidewall spacers on said stacked gate have a thickness of between about 1200 to 1500 Å.

38. (Previously Presented) A stacked gate memory cell pair of Claim 29, wherein said impurity implantation tilt angle is between about 40 to 50 degrees from the horizontal.